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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,430	05/05/2004	Hung-Lieh Hu	12898-US-PA	3429

31561 7590 08/31/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
GARCIA JR, RENE	
ART UNIT	PAPER NUMBER
2853	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,430	HU, HUNG-LIEH	
	Examiner	Art Unit	
	Rene Garcia, Jr.	2853	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-13,16-23 and 25-28* is/are rejected.

7)☒ Claim(s) *5,6,14,15 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05 May 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 26 June 2006. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 7, 8, 9, 10, 11, 16-20, 22 and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Hu et al. (US 2003/0030687).

Hu et al. discloses the following claimed limitations:

*regarding claims 1, 10, 22 and 25, inkjet printer identification circuit/**75/**, for providing a content stored in an inkjet print head/**62/** for an inkjet printer/**50/** (paragraph 0028), said inkjet print head/**62/** disposed inside said inkjet printer/**50/**, comprising: (fig. 5 & 7; paragraphs 0026-0028)

*plurality of control lines/**power supply lines, 82/** (fig. 7; paragraph 0031)

*control circuit/**76/** (fig. 7), providing a control signal to said plurality of control lines/**82/** (paragraph 0031)

*identification module/**recognition circuit, 70/** (fig. 7), including an identification unit/**75/**, said identification unit/**75/** including at least a control input terminal/**first end, 85/** (fig. 11; paragraph 0031)), an output terminal/**signal transmission line, 79/** (fig. 7 & 11; paragraph 0030 & 0031) and at least a data input terminal/**common output end, 89/**, said data input

terminal/**89**/ being coupled to a memory unit/**identifying cell, 84**/ (fig. 11; paragraph 0030) for receiving a content stored in said memory unit (one-bit identification code is either "1" or "0"), said control input terminal/**85**/ being coupled to one of said plurality of control lines/**82**/, said identification unit/**75**/ responsive to said control signal for determining and outputting the content stored in said memory unit/**84**/ via said output terminal/**79**/ (paragraphs 0030 – 0032; control circuit/76/ applies a voltage to power line/82/ connected to identifying cell/84/ storing desired data)

*regarding claims 2, 11 and 20, memory unit/**identifying cell, 84**/ includes a fuse/**87**/ (fig. 11; paragraph 0030)

*regarding claim 7, identification module/**recognition circuit, 70**/ is electrically coupled to said control circuit via a transmission line/**signal transmission line, 79**) (fig. 7 & 11; paragraph 0030 & 0031)

*regarding claims 8, 18 and 27, plurality of control lines is power supply lines/**82**/ (paragraphs 0030 & 0031)

*regarding claims 9, 17 and 26, plurality of control lines is address lines/**48A**/ (figs. 1 & 4; paragraphs 0004, 0006, 0007 & 0035)

*regarding claims 16 and 25, inkjet printer identification method comprising:

*using at least one control signal/**power supply line, 82**/ provided to an identification unit to read a content stored in at least a memory unit/**identifying cell, 84**/, wherein said memory unit/**84**/ is read via said identification unit/**identification circuit, 75**/ based on an arrangement of

a signal level of said control signal (fig. 7 & 11; paragraphs 0026 – 0032: identifying voltage is applied instead of working voltage/VP/), wherein said control signal is logically operated with said content to obtain an output signal (paragraph 0031; identifying voltage/control signal/ is applied to power supply lines/82/ and identifying cell/84/ responds by outputting either a "1" or "0" [logic output of memory unit]; claim recitation does not specify that control signal is a logic signal, only that control signal and memory unit operate with logically to output signal i.e. combination of providing identifying voltage to identifying cell results in a logical signal being output)

*regarding claims 19 and 28, content at least includes one of an ink cartridge product number, a number of inkjet nozzle, a volume of ink, a manufacturing date, a status of an ink cartridge, a type of an ink (paragraph 0028)

*further regarding claim 25, inkjet printer identification method characterized in using a control signal to read a content stored in one of a plurality of memory units/**identifying cell, 84/** (fig. 11; paragraph 0030)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (US 2003/0030687) in view of Dodd (US 2003/0063297).

Hu et al. discloses all the claimed limitations except for the following:

*regarding claims 3, 12 and 21, memory unit includes a low-power resistor

Dodd discloses the following:

*regarding claims 3, 12 and 21, memory unit**/ROM, 16A/** includes a low-power resistor**/310/** (fig. 3A; paragraphs 0018-0020, 0029 & 0032)

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to utilize a memory unit including a low-power resistor as taught by Dodd into Hu et al. for the purpose of blowing a fusible bit related to data of a memory structure of a print head.

6. Claims 4, 13 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hu et al. (US 2003/0030687) in view of Li (US 6,871,933).

Hu et al. discloses all the claimed limitations except for the following:

*regarding claims 4, 13 and 23, identification unit comprises a NAND gate, said NAND gate includes a plurality of NAND gate input terminals and a NAND gate output terminal, one of said plurality of NAND gate input terminals is coupled to said data input terminal, one of the other of said plurality of NAND gate input terminals is coupled to said control input terminal, said NAND gate output terminal is said output terminal of said identification unit

Li discloses the following:

*regarding claims 4, 13 and 23, identification unit comprises a NAND gate**/logic unit, 430/**, said NAND gate includes a plurality of NAND gate input terminals and a NAND gate

output terminal, one of said plurality of NAND gate input terminals is coupled to said data input terminal, one of the other of said plurality of NAND gate input terminals is coupled to said control input terminal, said NAND gate output terminal is said output terminal of said identification unit (fig. 4; col. 7, lines 39 & 40; col. 4, line 64-23; see also col. 3, lines 14-21 & lines 28-36)

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to utilize an identification unit comprises a NAND gate, said NAND gate includes a plurality of NAND gate input terminals and a NAND gate output terminal, one of said plurality of NAND gate input terminals is coupled to said data input terminal, one of the other of said plurality of NAND gate input terminals is coupled to said control input terminal, said NAND gate output terminal is said output terminal of said identification unit as taught by Li into Hu et al. for the purpose of identifying the ink jet print head.

Response to Arguments

7. Applicant's arguments filed 26 June 2006 have been fully considered but they are not persuasive.

8. Applicant on page 13 (REMARKS; section identified as "2") argues that identifying cell/84/ of Hu et al. (US 2003/0030687) is "not the memory unit 230 of the present invention". Claim interpretation regarding memory unit recites that data input terminal is coupled to a memory unit and that memory unit has content stored. Identifying cell/84/ of Hu et al. teaches using a fuse to provide either a "1" or "0" upon providing a identifying voltage, and the "content" provides no further limitation on what or how much information is required therefore providing a "1" or "0" is sufficient to read on the claimed limitation.

9. Regarding the use of common output end/89/ as the data input terminal, common output end/89/ is the input to switch/92/ which in turn outputs the signal(s) provided from identifying cell(s)/84/ to control circuit/76/. In relation to pages 12 and 13 (REMARKS; section identified as "1") claim 1 recites limitations for identification unit and those in particular recite identification unit includes: control input terminal, output terminal, data input terminal. Claim 1 further recites that a memory unit is coupled to data input terminal. However no recitation is provided such that data input terminal is coupled to "input" of the memory unit or what the data input terminal is responsible for "receiving. Therefore the claim interpretation allows for data input terminal/**common output end, 89/** to receive the output of the memory unit(s)/identifying cell(s),84/ and thus be coupled to memory unit. The common output end/89/ of Hu et al. is a point of input to switch/92/ to be controlled by control circuit/76/ to output identification information to control circuit. Claimed limitations provide for broad interpretation since they fail to provide specific recitation to how each component is connected/coupled with relation to each other (i.e. data input terminal is coupled to input terminal of memory unit; output of memory unit is coupled to output terminal of identification unit or similar recitation to provide clarification).

10. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., data input terminal is not used for outputting the determined content (see REMARKS end of section "1" top of page 13; and third paragraph of section"2") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

11. Applicant in section "3" or pages 13 and 14 with regards to claims 16 and 25 makes reference to power supply line/82/ as the control signal. As a matter of clarification, power supply line/82/ carries the control signal, in Hu et al. the identifying voltage is the control signal provided. Further claim recites "control signal is logically operated with said content", [Hu et al. paragraph 0031] identifying voltage/control signal/ is applied to power supply lines/82/ and identifying cell/84/ responds by outputting either a "1" or "0" [logic output of memory unit]; claim recitation does not specify that control signal is a logic signal, only that control signal and memory unit operate with logically to output signal i.e. combination of providing identifying voltage to identifying cell results in a logical signal being output.

Allowable Subject Matter

12. Claims 5, 6, 14, 15 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: The primary reason for indicating allowable subject matter of claims 5 and 6 is the inclusion of the limitations of an inkjet printer including identification module comprises a plurality of identification units, each of said plurality of identification units comprises at least a control input terminal, an output terminal and a plurality of data input terminals, said plurality of data input terminals is coupled to a corresponding one of a plurality of memory unit respectively, said control input terminal is coupled to corresponding one of said plurality of control lines, said

identification units are responsive to said control signals received from said plurality of control lines for determining and outputting the content stored in at least one of said plurality of memory units via said output terminal. It is these limitations found in each of the claims, as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for indicating allowable subject matter of claims 14 and 15 is the inclusion of the limitations of an inkjet printer including identification module includes a plurality of identification units, each of said plurality of identification units includes at least a control input terminal, an output terminal and a plurality of data input terminals, said plurality of data input terminal is coupled to a corresponding one of a plurality of memory unit respectively, said control input terminal is coupled to corresponding one of a plurality of control lines, said identification units are responsive to said control signals received from said plurality of control lines for determining and outputting a content stored in at least one of said plurality of memory units via said output terminal. It is these limitations found in each of the claims, as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

The primary reason for indicating allowable subject matter of claim 24 is the inclusion of the method steps being for an inkjet printer that identification unit includes: a plurality of AND gates, each of said plurality of AND gates including a plurality of AND gate input terminals and an AND gate output terminal, one of said plurality of AND gate input terminals being coupled to one of said plurality of data input terminals, the other said plurality of AND gate input terminals being coupled to said control input terminal; and a NOR gate, including a plurality of NOR gate

input terminals and a NOR gate output terminal, each of said plurality of AND gate output terminals being coupled to one of said plurality of NOR gate input terminals, said NOR gate output terminal being said output terminal of said identification unit. It is these steps found in each of the claims, as they are claimed in the combination, that has not been found, taught or suggested by the prior art of record which makes these claims allowable over the prior art.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communications with the USPTO

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rene Garcia, Jr. whose telephone number is (571) 272-5980. The examiner can normally be reached on M-F 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen D. Meier can be reached on (571) 272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Rene Garcia Jr
08/06

STEPHEN MEIER
SUPERVISORY PATENT EXAMINER